WBS 6.6.x.4
MDT Hit Extractor Boards and Firmware

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NSF Conceptual Design Review of the U.S. ATLAS HL-LHC Upgrade
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Bio-Sketch

- Verena Martinez Outschoorn
  - Assistant Prof. at U. of Illinois Urbana-Champaign, Summer-2014
  - ATLAS member 2006-2011 and 2014-Present
    - PhD Harvard U.
      - Main focus of work was on construction, commissioning and integration of MDT chambers & electronics
    - Faculty
      - Currently working on New Small Wheel trigger processor upgrade
        - → similar technology to this proposal
  - CMS 2011-2014
    - Lederman fellow at Fermilab (postdoc)
  - Searches for exotic physics with Higgs bosons

Institute Overview

- U. of Illinois Urbana-Champaign
  - ATLAS institute since 1994
    - Historically involved in Tile calorimeter, Muons, TDAQ and Computing
  - Electronics shop at Illinois
    - Experienced engineers and technician in board design, firmware development, testing of fixtures, assembly and production
    - Current ATLAS projects:
      - SSB board for ATLAS FastTracKer (FTK)
      - Trigger Processor for the New Small Wheel (NSW)
    - Previous experience on trigger electronics for CDF, Mu2e and DES
  - 4 professors (Steve Errede, Ben Hooberman, Mark Neubauer and VMO)

Outline WBS 6.6.x.4

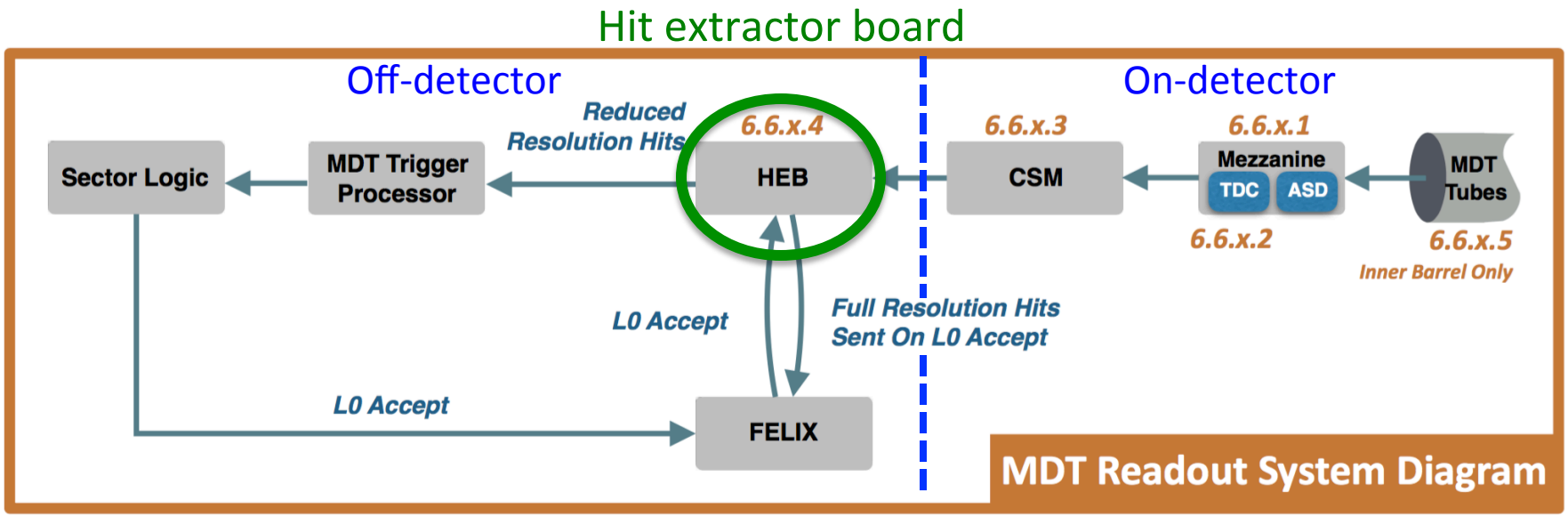
- Engineering, fabrication and testing of the Hit Extractor Boards for the MDT detectors. Includes firmware development.

- Deliverables
  - Hardware to operate the Hit Extractor system
    - 2 ATCA crates with 24 Hit Extraction Boards: 4 mezzanine cards, 1 carrier card and 1 rear transition module, RTM
    - 10% spare boards assumed in the estimate.
  - Firmware to operate the hardware with the desired functionalities.
  - Integration and testing in fully loaded crates.

- US Institute: University of Illinois Urbana-Champaign

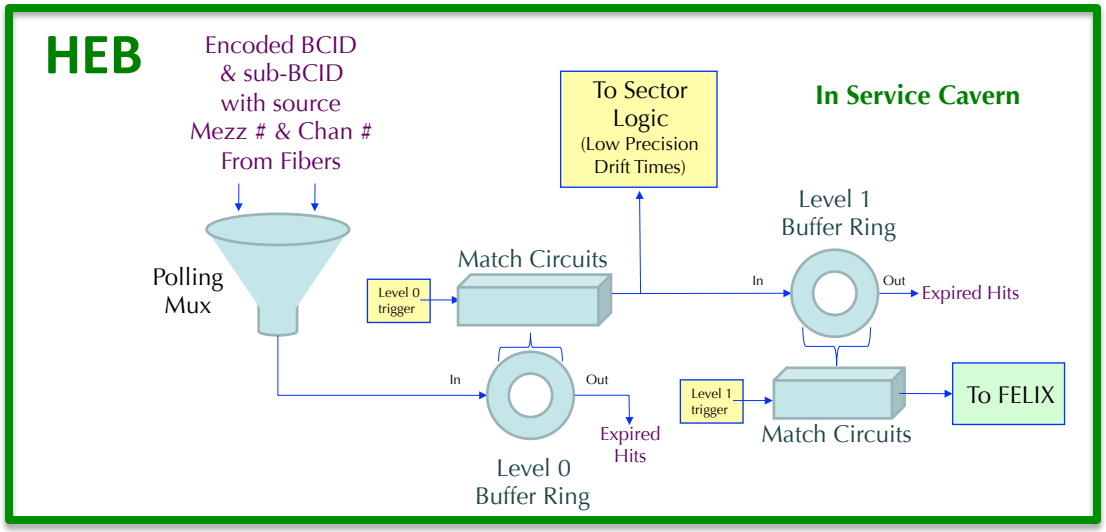
Proposed MDT Readout Scheme

- Reading out all the data to USA15 is an attractive option
  - Prompt availability of data for the trigger
  - Simple design, complexity reduced in on-chamber electronics
  - "Read all" scheme is possible with lower bandwidth needs.
    - Due to the long drift time of 40 bunches crossings, every MDT hit is read out at the L0 rate of 1MHz. At this L0 rate, headers that specify the event information occupy significant bandwidth. In a "read all" scheme, all hits are read off the MDTs as soon as available. The L0 event information is assigned to hits in the HEB, saving bandwidth.



Hit Extractor Board Functions

- Functions of the Hit Extractor Board (HEB)
  - Receive the digitized leading and trailing edge times from the CSMs.
  - Provide data buffering for trigger/DAQ latencies.
  - Provide data processing for event building and trigger.
  - Deliver low-latency, low-granularity signals to the hardware trigger.
  - Interface with the network-based trigger/DAQ system (FELIX).
  - Provide configuration and monitoring capabilities.

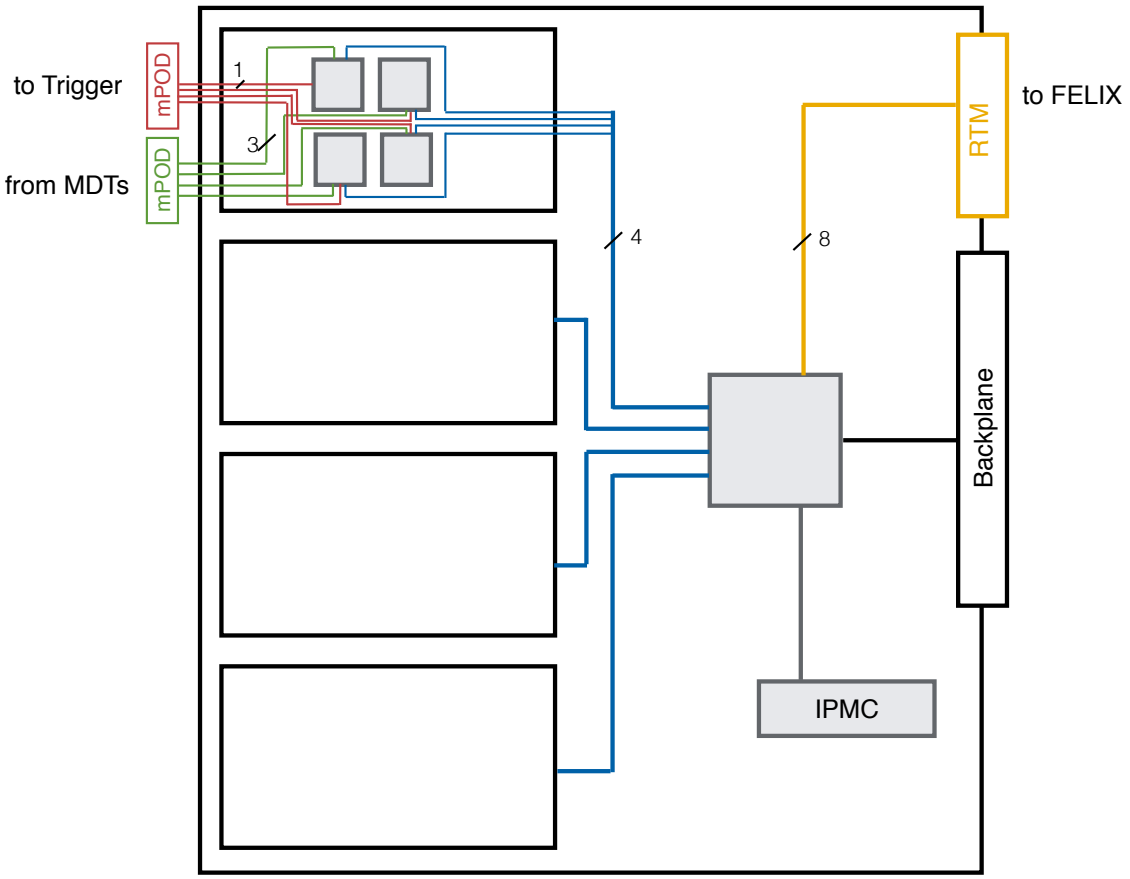


Motivation for Proposed U.S. Scope

- The MDT readout chain is primarily a US project
  - The US will be responsible for most of the electronics
  - The HEB completes the chain
- Historically, the US has been responsible for the MDT electronics, including several functionalities of the HEB
  - There is a lot of experience in the community
- The HEB is a good match to the skills and interests of the proposed group (University of Illinois, Urbana-Champaign)
  - Experienced engineers in high speed digital electronics and firmware development
  - Experienced physicist manpower
- Delivers high impact component of the HL-LHC upgrade for the ATLAS Muons.

Proposed Hardware Implementation

- Possible Implementation in ATCA platform
  - 24 ATCA blades (+ spares)
    - 4 Mezzanine cards, each process 12 input channels
    - 1 Carrier card
    - 1 RTM
  - Full system with ~1100 input channels fits in 2 ATCA crates – compact
- ATCA platform proposed in ATLAS for Phase-II



Advantages of Design

- Reduced dependence on on-chamber electronics
  - Without the Hit Extractor boards, the functionalities, including data buffering, would occur on the detector.
  - On-chamber electronics cannot be easily accessed and are higher risk in case of failures
- Greater flexibility
  - This design moves as much of the readout electronics into the service cavern as possible
  - Increases the flexibility in operation
    - Important because these systems usually work for longer than the initial design.
    - Unexpected situations are easier to address with commercial FPGA based readout systems, compared to designs that are more dependent for example on ASICs, which are more rigid (e.g. changes in the cavern background, etc)
  - Increases the possibilities for future updates or system upgrades

Research & Development

- Main tasks for R&D effort:
  - Detailed engineering design of the hardware
  - Simulation of the system
  - Measurement of system performance on evaluation boards

- Challenges to be addressed by R&D effort:
  - The size of the system depends on several factors including the number of channels and the processing needs, which affect the choice of FPGA. The system requirements need to be finalized, depending also on the choice of Trigger/DAQ scheme in ATLAS.
  - Another issue that can significantly increase the complexity of the readout is the possibility of using legacy electronics due to the difficult access to some of the chambers in the muon barrel.

HEB Schedule

- FY17-20: R&D
  - FY16-17: develop simulation and investigate hardware platforms (target TDR).
  - FY18-20: Detailed engineering design of the hardware and preliminary measurements of system performance on test hardware.
- FY 20-21: Preproduction. Final prototypes.
- FY 22-24: Production phase.

Budget Estimation

- Material costs
  - Costs for parts are determined from parts distributors.
    - Justification of components is provided in the BOE.
    - The estimate uses current costs, without scaling for inflation nor taking into account the availability of newer technologies that are expected to reduce the cost.
  - Assembly costs are estimated from previous experience with similar projects at Illinois.
  - Test stand costs are estimated using a recently purchased test stand.

- Personnel costs
  - Labor rates assumed are based on the manpower available at the U. of Illinois Urbana-Champaign
    - Support requested for senior engineer and technician
    - Includes fringe and overhead.

Risk

- Schedule
  - Potential problems: support and availability for technically experienced manpower (engineers and technicians).
  - Mitigation: Begin support for R&D activities as soon as possible.
- Cost
  - Potential problems: Cost is driven by the size of the system to be built, the choice of FPGAs and the assembly costs.
  - Mitigation: Perform R&D studies to provide a detailed system design.
  - Current top-down Muon contingency estimate is sufficient to cover possible system changes → safe cost estimate. More detailed bottom-up risk/contingency assessments are being prepared.
- Technical/Scope
  - Potential problems:
    - The size of the system (number of channels, FPGA choice, etc).
    - Readout of legacy electronics.
  - Mitigation: Begin R&D studies of the performance of the proposed design and possible alternatives as soon as possible.

Backup

Cost Estimate Summary

6.6.4.4 HEB - Illinois						
WBS	Description	Labor FTE	Labor Ayk$	M&S Ayk$	Travel Ayk$	TOTAL Ayk$
	Design/Prototype	**2.0**	**322**	**10**	**10**	**342**
	Engineers	1.0				
	Techs	1.0				
	Pre-Production	**2.0**	**332**	**10**	**10**	**352**
	Engineers	1.0				
	Techs	1.0				
	Production & Testing	**4.0**	**693**	**773**	**20**	**1,486**
	Engineers	2.0				
	Techs	2.0				
6.6.4.4	**HEB_Illinois**	**8.0**	**1,347**	**793**	**40**	**2,180**
	Engineers	4.0				
	Techs	4.0				

Labor Request

- Labor request
  - Request to support experienced senior engineer and technician available at UIUC.
  - Physicist manpower includes V. Martinez Outschoorn, who has 5 years of dedicated experience on MDTs, a postdoc and several students.
- Timeline of activities
  - FY17-20: R&D.
  - FY 20-21: Preproduction. Final prototypes.
  - FY 22-24: Production.